IN THE SPECIFICATION:

Please amend paragraph **[0001]** as follows:

[0001] This application is a divisional of application Serial No. 10/414,147, filed April 15, 2003, ~~pending.~~ now U.S. Patent No. 6,740,392, issued May 25, 2004.

Please amend paragraph **[0029]** as follows:

[0029] The top barrier layer 28 may be formed over a top surface of the dielectric layer 18 and the metallization layer 24. While the top barrier layer 28 is illustrated as a single layer, the top barrier layer 28 may, in actuality, include multiple portions. For instance, a portion of the top barrier layer 28 above the metallization ~~layer~~ layer 24 may be conductive while a portion of the top barrier layer 28 above the dielectric layer 18 may be nonconductive.

Please amend paragraph **[0030]** as follows:

[0030] The top barrier layer 28 of the semiconductor device ~~structure~~ structure 2 may be formed on a top surface of the semiconductor device structure 2. FIGS. 2A-2E show cross-sectional views of the semiconductor device structure 2 fabricated according the present invention. FIG. 2A illustrates a portion of the semiconductor device structure 2 having a number of semiconductor devices 6, 8. The semiconductor devices 6, 8 may be formed in the semiconductor substrate 4 and include active semiconductor devices 6, such as transistors, and passive semiconductor devices 8, such as capacitors, or a combination of active and passive semiconductor devices 6, 8. The semiconductor device structure 2 optionally includes the protective layer 10, which is deposited over the semiconductor substrate 4 and semiconductor devices 6, 8. The protective layer 10 may be formed from Si_3N_4 and deposited at a thickness of about 100 nm. The dielectric layer 18 may be deposited over the protective layer 10. However, it is also contemplated that the dielectric layer 18 may be formed before the protective layer 10 and, therefore, may be present under the protective layer 10. The thickness of the dielectric layer 18 may depend on the material that is used. For instance, if the dielectric layer 18 is formed from a polymer, the polymer may be deposited to a sufficient thickness to equal a desired

thickness of a first wiring level when the polymer is cured. If the dielectric layer 18 is formed from SiO_2, SiO_2 may be deposited to a thickness that is equal to the desired thickness of the first wiring level.

Please amend paragraph **[0039]** as follows:

[0039] The process described above may be utilized to form a single damascene structure. A dual damascene structure may be constructed using appropriate masking steps known in the art. It is also contemplated that the process may be repeated to form a desired number of metallization ~~layers~~ layers 24 in the semiconductor device structure 2.

Please amend paragraph **[0041]** as follows:

[0041] In one embodiment of the present invention, a semiconductor device structure 2 using copper metallurgy in its entire wiring pattern is formed. A layer of about 100 nm of Si_3N_4 is, optionally, deposited over the semiconductor substrate 4 and semiconductor devices 6, 8 to form the protective layer 10. The dielectric layer 18, formed from polyimide, is then deposited over the protective layer 10 and cured. The polyimide layer is of sufficient thickness so that its thickness equals the first contact and wiring level of the semiconductor device structure 2 when the polyimide is cured. Contacts 12 are then opened through the polyimide layer and the protective ~~layer.~~ layer 10. TiN is deposited to form the first barrier layer 14 and W is deposited to form the metal plug 16. Excess W and TiN are subsequently removed from the surface of the protective layer 10 or the polyimide layer by CMP.

Please amend paragraph **[0044]** as follows:

[0044] In another embodiment, the dielectric layer 18 is formed from SiO_2. A layer of approximately 100 nm of Si_3N_4 is, optionally, deposited over the semiconductor substrate 4 and semiconductor devices 6, 8 to form the protective layer 10. In this embodiment, the dielectric layer 18, formed from SiO_2, is formed over the Si_3N_4 layer. Contacts 12 are then opened through the SiO_2 layer and the protective ~~layer.~~ layer 10. TiN is deposited to form the first barrier

layer 14 and W is deposited to form the metal plug 16. Excess W and TiN are subsequently removed from the surface of the protective layer 10 or the SiO_2 layer by CMP. An additional oxide layer is then applied having a thickness equal to the desired thickness of the first wiring level.